CLAIMS

1. A error detection system for a clock signal comprising:

a first counter that receives and counts the clock signal,

a phase-locked loop circuit that receives the clock signal and outputs a second clock signal,

a second counter that receives and counts the second clock signal, and

a comparator that receives and compares the outputs of the first and the second counters, and

an error output from the comparator that is true when the counts of the first and the second counters are unequal.

2. The error detection system as defined in claim 1 further comprising and second output from the comparator that indicates which counter contains a higher count.

3. The error detection system as defined in claim 1 further comprising means for re-setting the counters synchronized to the successful capture of the clock signal by the PLL.

4. The error detection system as defined in claim 1 further comprising:

a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal,

a receiver latch that accepts and latches the data therein with the forwarding clock.

5. A method for detecting clock signal errors comprising the steps of:

a first counting of the first clock signals,

providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal,

a second counting of the second clock signals,

detecting a difference between the first and the second countings, and

signaling an error therewith.

6. The method as defined in claim 5 further comprising the step of: signalling which counting is higher.

7. The methods as defined in claim 5 further comprising the step of synchronizing the two countings.

8. The method as defined in claim 5 further comprising the steps of:

sending data and the clock signal, wherein the clock signal is a forwarding source synchronous clock signal,

receiving the data, and

latching the data with the forwarding clock signal.